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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,071	09/23/2003	Karim-Thomas Taghizadeh-Kaschani	WMP-IFT-965	2703

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/669,071	TAGHIZADEH-KASCHANI, KARIM-THOMAS	
	Examiner	Art Unit	
	Emmanuel Bayard	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-9 and 11-12* is/are rejected.

7)☐ Claim(s) *5,6,13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendments filed on 10/22/07 in which claims 1-9 and 11-14 are pending. The applicant's amendments have been fully considered but they are moot based on the new ground of rejection.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 7-9 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salamina et al U.S. Patent No 5,541,541 in view of Nakagawa U.S. Pub No 20010026490 A1.

As per claims 1 and 8, Salamina et al teaches a receiver circuit for a push-pull transmission method, comprising: at least one first input for receiving a first input signal (see figs.3-4 element A); at least one second input for receiving a second input signal (see figs.3-4 element B); an output providing an output signal dependent on the first and second input signals (see figs.3-4 element 11); a detector circuit having a first signal detector connected to said first input (see figs. 3-4 elements COMP1, 16 and col.2, lines 55-67) and a second signal detector connected to said second input (see figs.3-4 elements COPM2, 18), said first and second signal detectors comparing amplitudes of the first and second input signals in each case with a detection threshold and providing detector output signals including a first detector output signal from said first signal

detector and a second detector output signal from said second signal detector (see col.3, lines 16-67 and col.4,lines 1-45) said first and second signal detectors each having a control input for setting the detection threshold, said control input of said first signal detector being coupled to an output of the second signal detector and said control input of said second signal detector being coupled to an output of said first signal detector (see figs.3-4 elements 20 and 22 and col.3,lines 31-67); and transistor is the same as the claimed (signal processing circuit) connected to said detector circuit and receiving the detector output signals, said signal processing circuit generating the output signal according to the detector output signals (see figs. 3-4 elements 12 and 14 and col.3, lines 25-30).

However Salamina et do not teach setting the detection threshold to at least a first value and a second value lower than the first value after an amplitude of one of the first and second input signals exceeds the first value of the detection threshold, the detection threshold compared to another one of the first and second input signals being decreased to the second value of the detection threshold.

Nakagawa teach setting the detection threshold to at least a first value and a second value lower than the first value after an amplitude of one of the first and second input signals exceeds the first value of the detection threshold, the detection threshold compared to another one of the first and second input signals being decreased to the second value of the detection threshold (see page 1 [0011]).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Nakagawa into Salamina as to determine whether the output voltage would

be high or low as taught by Nakagawa (see page 1 [001]).

As per claim 2, Salamina et al teach wherein said first and second signal detectors have a first detection threshold or a second detection threshold according to a signal present at said control input (see figs.3-4 elements 20 and 22 and col.3, lines 31-67).

As per claim 3, Salamina et al inherently teaches, wherein said first and second signal detectors are trigger with an adjustable upper switching threshold (see col.5, lines 40-50). Furthermore implement such teaching in the combination of Salamina and Nakagawa would have been obvious to one of ordinary skill in the art to implement the teaching of Nakagawa into Salamina as to determine whether the output voltage would be high or low as taught by Nakagawa (see page 1 [001]).

As per claim 7, Salamina et al teaches, wherein said first and second inputs are two of a plurality of inputs connected to said detector circuit, said detector circuit having a plurality of signal detectors each connected to one of said inputs, said control input of a respective one of said signal detectors having applied to it a signal dependent on output signals of other ones of said signal detectors (see figs. 3-5).

As per claim 9, Salamina et al and Nagkagawa in combination would teach further comprises increasing the detection threshold to the first value for comparing with the one signal after the other signal has reached the detection threshold having a third value as to accurately determine whether the output voltage would be high or low as taught by Nakagawa (see page 1 [001]).

As per claim 11, Salamina et al and Nagkagawa in combination would teach

which further comprises setting the third value to be less than the first and second values as to accurately determine whether the output voltage would be high or low as taught by Nakagawa (see page 1 [001].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Salamina et al U.S. Patent No 5,541,541 in view of Nakagawa U.S. Pub No 20010026490 A1 and in further view of Lenz U.S. patent No 4,953,070.

5. As per claim 4, Salamina and Nakagawa in combination teach all the features of the claimed invention except wherein said signal processing circuit has an edge spacing evaluation unit for detecting predetermined edges of the detector output signals and provides further output signals dependent on the detector output signals and on a temporal spacing between a predetermined edge of the first detector output signal and a predetermined edge of the second detector output signal.

As per claim 4, Lenz teaches wherein said signal processing circuit has an edge spacing evaluation unit for detecting predetermined edges of the detector output signals and provides further output signals dependent on the detector output signals and on a temporal spacing between a predetermined edge of the first detector output signal and

a predetermined edge of the second detector output signal (see abstract and col.1, lines 13-15 and col.2, lines 48-53 and col.3, lines 1-15 and col.6, lines 36-39).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Lenz into the combination of Salamina and Nakagawa as to detect the output current of the output transistor arrays which comprise releasing the particular triggering push-pull signal for an output transistor array without delay whenever the output current of the complementary transistor arrays drops below a predetermined of a positive minimum value as taught by Lenz (see col.2, lines 48-55)

Allowable Subject Matter

1. Claims 5-6 and 13-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571 272 3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

1/3/2008

Emmanuel Bayard
Primary Examiner
Art Unit 2611

EMMANUEL BAYARD
PRIMARY EXAMINER

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